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10/552,601	10/05/2005	Chung Kuang Chin	Terablaze 4	6402

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EXAMINER	
HO, CHUONG T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,601	CHIN ET AL.	
	Examiner	Art Unit	
	CHUONG T. HO	2476	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed 06/21/10*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1-8,18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/21/10 has been entered.

2. The amendment filed 06/21/10 have been entered and made of record.

Response to Arguments

3. Applicant's arguments filed 06/21/10 have been fully considered but they are not persuasive.

Independent Claims 1 and 18

In Page 7, Lines 6-10, the applicant argues that Neither Muller nor Sindhu, alone or in combination, disclose or suggest that a shared memory comprises two or more buffers and two or more banks; wherein each of the banks comprises portions, wherein each of the two or more buffers comprises a portion from each of the plurality of banks, and wherein each of the buffers identifies an address of a location in each Of the banks.

The examiner respectfully disagrees with the applicant's argument.

Muller '132 teaches shared memory comprises two or more buffers (i.e., buffer #1, buffer #2, buffer #3) [see figure 3A] (i.e., a logical view of **shared memory** 230 is depicted having stored therein packet data in a number of buffers. In this example, the **shared memory** 230 is segmented into a number of buffers (pages) of programmable size. All the buffers may have the same size, or alternatively, individual buffer sizes may vary) [col. 8, lines 37-42, Referring now to FIG. 3A] (i.e., a portion of the received packets may be buffered temporary) [see col. 7, lines 7] in contiguous banks (i.e., banks = buffer #1, buffer #2, buffer #3) [see Fig. 3A] of a first buffer (i.e., shared memory 230) [see figure 3A].

Sindhu '660 teaches shared memory comprises two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) [see Fig. 9], at least a portion of packet in contiguous banks (i.e., banks 902) [see Fig. 9] of a first buffer (M (0) of said two or more buffer (M (0), M (1), M (2).. M(7)), wherein each of said banks (i.e., banks 902) [see Fig. 9] comprises portions, wherein each of said two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) comprises a portion from each of said plurality of banks figure 9, banks 902) [see Fig. 9] , and wherein each of said buffers identifies an address of a location in each of said banks (i.e., each memory bank has a unique 3 bit physical band number, or PBN, that is equal to the number of the slot in which the bank is plugged) [see col. 14, lines 30-35].

Thus, Muller '132 and Sindhu '660 teach wherein said shared memory comprises two or more buffers and two or more banks, at least a portion of a packet in contiguous banks of a first buffer of said two or more buffers, wherein each of said banks comprises portions, wherein each of said two or more buffers comprises a portion from each of said plurality of banks, and wherein each of said buffers identifies an address of a location in each of said banks, as required by independent claims 1 and 18.

4. Claims 1-8, 9-13, 18-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 7-8, 18, 21, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al. (Hereafter Sindhu '660) Patent No.: 7,116,660 B2.

Regarding to claim 1, Muller '132 teaches a method for storing (i.e., stored therein packets) [see Fig. 3A and Col. 8, Lines 37-39] in a shared memory (i.e., shared

memory) [see Col. 8, Lines 37-39] in a packet switch (i.e., switching fabric) [see Fig. 2] , said shared memory comprising two or more buffers (i.e., shared memory comprises buffer #1, buffer #2, buffer #3) [see figure 3A], said method comprising the step of:

- storing in said shared memory, wherein said shared memory comprises two or more buffers (i.e., buffer #1, buffer #2, buffer #3) [see figure 3A] (i.e., a logical view of **shared memory** 230 is depicted having stored therein packet data in a number of buffers. In this example, the **shared memory** 230 is segmented into a number of buffers (pages) of programmable size. All the buffers may have the same size, or alternatively, individual buffer sizes may vary) [col. 8, lines 37-42, Referring now to FIG. 3A] (i.e., a portion of the received packets may be buffered temporary) [see col. 7, lines 7] in contiguous banks (i.e., banks = buffer #1, buffer #2, buffer #3) [see Fig. 3A] of a first buffer (i.e., shared memory 230) [see figure 3A].

Muller '132 teaches all the subject matter of the claim invention above with the exception of disclosing each of said one or more buffers comprising a plurality of banks.

Sindlhu '660, the same or similar fields of endeavor, disclose storing in said shared memory (figure 9, shared memory), wherein said shared memory comprises two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) [see Fig. 9], at least a portion of packet in contiguous banks (i.e., banks 902) [see Fig. 9] of a first buffer (M (0) of said two or more buffer (M (0), M (1), M (2).. M(7)), wherein each of said banks

(i.e., banks 902) [see Fig. 9] comprises portions, wherein each of said two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) comprises a portion from each of said plurality of banks figure 9, banks 902) [see Fig. 9] , and wherein each of said buffers identifies an address of a location in each of said banks (i.e., each memory bank has a unique 3 bit physical band number, or PBN, that is equal to the number of the slot in which the bank is plugged) [see col. 14, lines 30-35]

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the data buffer 104 includes two or more memory banks, the data packet is divided among the memory banks as taught by Sindlhu '660 in the shared memory of Muller '132. The data buffer 104 includes two or more memory banks, the data packet is divided among the memory banks can be implemented / modified the shared memory of Muller '132 by using the shared memory (figure 3A) to perform. The motivation for using the data buffer 104 includes two or more memory banks, the data packet is divided among the memory banks as taught by Sindhu'347 into the shared memory of Muller '132 being that it allows the memory to be read and written conveniently (Sindhy, col. 4, line 9).

Regarding to claim 4, Muller et al. discloses wherein at least a portion (i.e., portions of packet #1, portions of packet #2) [see col. 7, line 7] of each of two or more packets are stored in one of said buffers (i.e., 350, buffer #1 stored portions of packet #1) [see figure 3A] (i.e., 360, buffer #1 stored portion of packet #2) [see figure 3A] (i.e., 351, buffer #2

stored portions of packet #1) [see figure 3A] (i.e., 361, buffer #2 stored portions of packet #2) [see figure 3A].

Regarding to claim 7, Muller et al. discloses wherein said shared memory exchanges packets between ports (between input ports and output ports) in said packet switch (i.e., After a forwarding decision is received for a particular packet, the **input port** 206 transfers ownership of the one or more buffers corresponding to the packet to the appropriate **output port**(s) 206. The transfer of ownership includes the **input port** 206 notifying the **shared memory** manager 220 of the number of output ports 206 that should transmit the packet and the **input port** 206 forwarding the appropriate pointers to those output ports 206) [see col. 7, lines 12-15].

Regarding to claim 8, Muller '132 packets are stored in contiguous banks (i.e., buffers comprise number of memory lines) [see col. 8, lines 43-44] of at least one of said two or more buffers (i.e., buffer #1, buffer #2, buffer #3) [see figure 3A]; however, Muller et al. are silent to disclosing wherein said sequential data units of said packet are stored in contiguous banks of at least one of said one or more buffers.

Sindlhu '660 disclose wherein said sequential data units of said packet are stored in at least one of said one or more buffers (i.e., Let the cells generated by a given stream be numbered I, I +1, I +2, ….etc. As was described above, cells are written to sequentially increasing bank number I mod b) [see col. 22, lines 40-45] (i.e., the distributed memory includes two or more memory banks, Each memory bank is used for

storing uniform portions of a data packet received from source and linking information of a data packet to allow for the extraction of the uniform portions of a data packet from distributed location in memory in proper order) [see Abstract].

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein said sequential data units of said packet are stored in at least one of said one or more buffers taught by Sindlhu '660 into the system of Muller '132 in order to allow the memory to be read and written conveniently (Sindhy, col. 4, line 9).

Regarding to claim 18, Muller '132 disclose a shared memory for storing a packet (i.e., shared memory 230 is depicted having stored therein packet data in a number of buffers) [see col. 8, lines 38-39] , comprising:

- Two or more buffer (figure 9, ,(i.e., shared memory includes buffer #1, buffer #2, buffer #3) [see figure 3A] (i.e., a logical view of **shared memory** 230 is depicted having stored therein packet data in a number of buffers. In this example, the **shared memory** 230 is segmented into a number of buffers (pages) of programmable size. All the buffers may have the same size, or alternatively, individual buffer sizes may vary) [see col. 8, lines 37-42, Referring now to FIG. 3A] (i.e., a portion of the received packets may be buffered temporary) [see col. 7, lines 7] in contiguous banks (i.e., banks = buffer #1, buffer #2, buffer #3) [see see figure 3A] of a first buffer (i.e., shared memory 230) [see figure 3A].

However, Muller '132 does not explicitly teach each of said buffers comprising a plurality of banks, wherein at least a portion of said packet is stored in contiguous banks of a first bufferr of said two or more buffers.

Sindlhu '660, the same or similar fields of endeavor, disclose storing in said shared memory (i.e., shared memory) [see figure 9], wherein said shared memory comprises two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) [see figure 9] , at least a portion of packet in contiguous banks (i.e., banks 902)[see figure 9] of a first buffer (M (0) of said two or more buffer (M (0), M (1), M (2).. M(7)), wherein each of said banks (i.e., banks 902) [see figure 9] comprises portions, wherein each of said two or more buffers (i.e., M (0), M (1), M (2), M(3) M(4) M(5) M(6) M(7)) [see figure 9] comprises a portion from each of said plurality of banks figure 9, banks 902) , and wherein each of said buffers identifies an address of a location in each of said banks (i.e., each memory bank has a unique 3 bit physical band number, or PBN, that is equal to the number of the slot in which the bank is plugged) [see col. 14, lines 30-35].

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the data buffer 104 includes two or more memory banks, the data packet is divided among the memory banks as taught by Sindlhu '660 in the shared memory of Muller '132. The data buffer 104 includes two or more memory banks, the data packet is divided among the memory banks can be implemented / modified the shared memory of Muller '132 by using the shared memory (figure 3A) to perform. The motivation for using the data buffer 104 includes two or more memory

banks, the data packet is divided among the memory banks as taught by Sindhu'347 into the shared memory of Muller '132 being that it allows the memory to be read and written conveniently (Sindhy, col. 4, line 9).

Regarding to claim 21, claim 21 is rejected the same reasons of claim 4 above.

Regarding to claim 23, claim 23 is rejected the same reasons of claim 7 above.

6. Claims 2, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al. (Hereafter Sindhu '660) Patent No.: 7,116,660 B2 and further in view of Benson et al. (Hereafter, Benson '321) Patent No.: 6,151,321.

Regarding to claim 2, Muller '132 and Sindhu '660 teach the limitations of claim 1 above.

Muller '132 further teaches wherein said packet (packet #1) comprises a plurality of portions (portions of packet #1) , and further comprising the step of storing an portion of said packet in contiguous banks of buffer (figure 3A, shared memory 230).

However, Muller '132 – Sindhu ' do not explicitly teach said data unit stored in said last bank of said first buffer is not a last data unit of said packet.

Benson '321, as the same or similar fields of endeavor, teaches the received shared memory pool mechanism 120 includes a first received shared memory pool 136

and second received shared memory pool 138. Each receive shared memory pool has receive local buffers 122 (see col. 5, lines 40-42) (col. 5, line 48-49, two or more pools allows for the advantage of multiple bank typically built into memory device);
comprising:
The step of storing an additional portion (the rest of the cell of the packet) of said packet in a second buffer (the second card buffer) if one of said portions (the cell of the packet) is stored in said first buffer (the first card buffer) and said portions stored in said first buffer (the first card buffer) is not a last portion of said packet (figure 7B, place enough data in the first card buffer to fill the host buffer, place the rest of the cell into the second card buffer).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate storing an additional portion of said packet in a second buffer if one of said data units is stored in said first buffer and said data unit stored in said first buffer is not a last unit of said packet taught by Benson '321 into the combined system (Muller '132 – Sindhu '660) in order to desire to utilize a dynamic packet memory management scheme to facilitate sharing of a common packet memory among all input / output ports for packet buffering (see Muller et al. col. 2, lines 16-17).

Regarding to claim 19, claim 19 is rejected the same reasons of claim 2 above.

7. Claims 3, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al.

(Hereafter Sindhu '660) Patent No.: 7,116,660 B2 and further in view of Kamaraj et al. (Hereafter, Kamaraj '757) Patent No.: 6,501,757.

Regarding to claim 3, Muller '132 and Sindhu '660 teach the limitations of claim 1 abvoe.

Muller '132 further teaches one or more buffer in shared memory; two or more buffer comprising a plurality of banks (col. 8, line 43, the buffers may be further subdivided into a number of memory lines); however, Muller '132 and Sindhu '660 do not explicitly teach wherein each of said one or more buffers comprises one or more group and each of said groups comprises a plurality of banks.

Kamaraj '757, in the same or similar fields of endeavor, teaches wherein each of said two or more buffers comprises one or more group and each of said groups comprises a bank (col. 7, lines 41-42, said cell buffer being housed in a shared cell buffer pool "buffer" organized as a bank of a plurality of groups.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein each of said one or more buffers comprises one or more group and each of said groups comprises a bank taught by Kamarau '757 into the combined system (Muller '132 – Sindhu '660) in order to provide efficient implementation of internal queue while also allowing configurability of speeds (Kamaraj, col. 6, lines 52-53).

Regarding to claim 20, claim 20 is rejected the same reasons of claim 3 above.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al. (Hereafter Sindhu '660) Patent No.: 7,116,660 B2 and further in view of Beshai (Hereafter, Beshai '448) Pub. No.: 2004/0184448.

Regarding to claim 5, Muller '132 and Sindhu '660 teach the limitations of claim 1 above.

Muller '132 further teaches each of said data port corresponding to one or more of said plurality of banks "buffers" (col. 8, lines 43-44, the buffers may be subdivided into a number of memory lines "banks") (col. 15, lines 1-2, a shared pool of packet memory and provides for efficient allocating of per port buffering that is proportional to the amount of traffic through a given port) ; however, Muller '132 and Sindhu '660 do not explicitly teach the step of cyclically accessing one or more data ports.

Beshai '448, in the same or similar fields of endeavor, teaches the step of cyclically accessing one or more data ports (page 1 paragraph [0005] the output rotor cyclically connects each transmit memory to each output port "data ports").

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the step of cyclically accessing one or more data ports taught by Beshai '448 into the combined system (Muller '132 – Sindhu '660) in order to desire to utilize dynamic packet memory management scheme to facilitate sharing of a common packet memory among all input / output ports for packet buffering (Muller, col. 2, lines 16-18).

9. Claims 6, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al. (Hereafter Sindhu '660) Patent No.: 7,116,660 B2 and further in view of Lavelle et al. (Hereafter, Lavelle '929) Patent No.: US 6,812,929.

Regarding to claim 6, Muller '132 and Sindhu '660 teach the limitations of claim 1 above.

Muller '132 further teaches allocating buffer in response to a buffer request (col. 10, lines 50-53, FIG. 5 is a flow diagram illustrating **buffer allocation** processing according to one embodiment of the present invention. At step 505, the next free buffer pointer is produced by the pointer generator 440. In one embodiment, the pointer generator 440 attempts to keep one or more pointers available to allow immediate servicing of buffer requests).

However, Muller '132 and Sindhu '660 do not explicitly teach wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set.

Lavelle '929, in the same or similar fields of endeavor, teaches wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set (col. 14, lines 59-62, a frame buffer, wherein the frame buffer includes a first set of one or more banks, a second set of one or more memory banks).

Thus, one would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set taught by Lavelle '929 into the combined system (Muller '132 – Sindhu '660) in order to improve the efficiency of accesses to the frame buffer so that rendering accesses may be performed more quickly (Lavelle, col. 2, lines 53-54).

Regarding to claim 22, claim 22 is rejected the same reasons of claim 6 above.

10. Claim 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (Hereafter, Muller '132) Patent No: 6,021,132 in view of Sindhu et al. (Hereafter Sindhu '660) Patent No.: 7,116,660 B2 and further in view Manning et al. (Patent Number: 6,088,736).

Regarding to claim 24, Muller '132 and Sindhu '660 teach the limitations of claim 18 above.

Muller '132 further teaches a method for managing a share memory (figure 2, figure 3, shared memory 230, col. 8, lines 37-38, the shared memory 230 is depicted having stored therein packet data in a number of buffers), said shared memory comprising one or more buffers (figure 3A, buffer #1, buffer #2, buffer #3), said method comprising the step of:

Maintaining a buffer usage count (see abstract, buffer usage count) for at least one of said buffers (Abstract, a shared memory manager for a packet forwarding device includes a pointer memory having stored therein information regarding buffer usage (e.g., usage **counts**) for each of a number of buffers in a shared memory) (col. 7, lines 25-27, The shared memory manager 220 then updates its internal **counts** used for tracking the number of buffer owners and returns the buffer to the free pool if appropriate (e.g., the buffer is no longer in any output queues)) (col. 9, lines 35-37, The buffer tracking unit 329 additionally includes a pointer random access memory (PRAM) 320. The PRAM 320 may be an on or off-chip pointer table that stores usage **counts** for buffers of the shared memory 230);

a counter for monitoring a buffer usage count (Abstract, Usage count) provides an indication of the input (write) over all packets in said at least one of said buffers of the number of output ports (two output ports) toward which each of said packet is destined (col. 12, lines 30-31, the other two output ports 206 complete transmission of the buffer and so notify the buffer tracking unit 329 Write "SUM" = 0010b) (col. 12, lines 27-30, The buffer tracking unit 329 processes the input port's 0010b notification which indicates there are 3 buffer owners. Read: 1110b Modify: 1110b + 0011b + 0001b = 0010b Write: 0010b The other two output ports 206 complete transmission of 0010b the buffer and so notify the buffer tracking unit 329);

wherein said at least one of said buffers contains two or more packets (see abstract, buffers for temporary buffering the packets).

However, Muller '132 and Sindhu '660 do not explicitly teach a sum over all packet in said at least one of said buffer.

Manning '736, as the same or similar fields of endeavor, teaches buffer usage count (col. 13, lines 15-25, tracking cells received at the upstream based upon observed buffer usage (buffer usage count)) (col. 13, lines 40-45, buffer usage data); comprising:

buffer provides an indication of the sum (col. 6, lines 20-35, total number of cells) over all packets in said at least one of said buffers of the number of output ports toward which each of said packets is destined, wherein said at least one of said buffers contains two or more packets (col. 6, lines 25-35, Buffer_counter 32 means sum of number of packets in the buffer) (col. 13, lines 15-25, tracking cells received at the upstream based upon observed buffer usage (buffer usage count)).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teaching of Manning '736 into the combined system (Muller '132 – Sindhu '660), since Manning '736 recited the motivation in the col. 1, lines 10-12, which is a joint flow control mechanism in a distributed switching architecture.

Allowable Subject Matter

11. Claims 9-13 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claim 9 is allowed over the prior art or record since the cited reference taken individually or in combination fails to particular disclose the following limitations: "adding said at least one of said buffers to a free buffer list if a release of said at least one of said buffers does not occur within a predefined period of time" and in combination with other limitations recited as specified in claim 9.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nation et al. (Hereafter, Nation '906) Patent No.: US 7,301,906 (i.e, If the received packet is stored in buffer memory dedicated to the specific port, element 208 may therefore represent processing to **increment** a counter representing usage of preallocated, dedicated storage per port. If the received packet is stored in shared buffer memory, element 208 may therefore represent processing to **increment** a counter representing usage of shared storage per port and also **decrementing** a second counter representing available shared storage. Conversely, element 212 represents processing to **increment or decrement** appropriate counters indicating freeing of a previously allocated buffer either allocated as dedicated memory associated with the port or allocated from shared memory for temporary use by a particular port) [see col. 10, lines 10-18].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571)272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sheikh Ayaz can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHUONG T HO/
Examiner, Art Unit 2476